

We Claim:

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1. A modular video processing system comprising:
a processing module containing at least one general purpose microprocessor
which controls hardware and software operation of said video processing system using
5 control data;

at least one video processing module which contains parallel pipelined video
hardware which is programmable by said control data to provide different video
processing operations on an input stream of video data;

10 a global video bus which routes video data between said processing module
and said at least one video processing module; and

a global control bus which provides said control data to/from said processing
module from/to said at least one video processing module separate from said video data
on said global video bus.

2. The system of claim 1, wherein said video data is coupled with
15 associated video timing information synchronized to a system clock, and each video
processing module comprises a crosspoint switch which routes said video data and its
associated video timing information to/from respective parallel pipelined video hardware
components, said timing data compensating for pipeline delay in said video processing
module.

20 3. The system of claim 2, wherein each video processing module further
comprises a crosspoint switch state machine which monitors transfers of video data over
each data path of said crosspoint switch and facilitates selection of idle data paths for
each transfer of data from one parallel pipelined video hardware component to another.

4. The system of claim 2, wherein at least one video processing module
25 comprises a configurable arithmetic logic unit (CALU) responsive to said video data
and its associated video timing information so as to automatically compensate for
differences in input video timing between respective images and to provide dual image
pointwise video processing operations and image accumulations.

5. The system of claim 2, wherein at least one video processing module comprises at least one pyramid filtering processor which generates pyramid representations of the video data at different resolutions so as to facilitate real-time processing of said video data for said particular image processing tasks of said video processing system.

6. The system of claim 2, wherein each video processing module comprises a connection for at least one daughterboard which performs a video processing function on said video data which is unique to particular image processing tasks of said video processing system.

10 7. The system of claim 6, wherein said at least one daughterboard comprises a display processor card including video input and output ports connected to said crosspoint switch and an encoder which converts video data received at an input port into a video signal of a predetermined format for display.

15 8. The system of claim 6, wherein said at least one daughterboard comprises a digitizer card including video input and output ports connected to said crosspoint switch and a decoder which decodes and digitizes video data received at an input port into a video signal of a predetermined format for further processing so as to provide an input and output interface for digital video.

20 9. The system of claim 6, wherein said at least one daughterboard comprises a correlator card including video input and output ports connected to said crosspoint switch and a plurality of video processing channels, each channel comprising a configurable arithmetic logic unit, a pyramid filtering processor, and a look up table which correlate respective images in each video processing channel in a predetermined manner.

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10. The system of claim 6, wherein said at least one daughterboard comprises a warper card including video input and output ports connected to said crosspoint switch and an address generator and a pair of memory banks for parametric transformation of video data received at an input port.

5 11. The system of claim 6, wherein said at least one daughterboard comprises a warper card including a plurality of video input and output ports connected to said crosspoint switch, a pair of memory banks, and a plurality of field programmable gate arrays programmed so as to provide parametric transformation of video data received at said input ports.

10 12. The system of claim 1, wherein said processing module comprises at least two microprocessors each of which has associated random access memory which is not shared with any other microprocessor, and shared memory which is accessible by each microprocessor of said processor module through an arbitrated control bus which arbitrates requests for said shared memory from each microprocessor.

15 13. The system of claim 12, wherein said processing module provides at least one synchronous start signal for each different video processing operation of each video processing module.

20 14. The system of claim 12, wherein said processing module further comprises communications devices for communicating with external devices, said communications devices being accessed by each of said microprocessors via said arbitrated control bus.

25 15. The system of claim 12, wherein said random access memory associated with each microprocessor is connected to said global video bus and stores video data for transmission to and stores video data received from said at least one video processing module over said global video bus.

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16. The system of claim 12, wherein said processor module further comprises a semaphore register available to each microprocessor via said arbitrated control bus, said semaphore register storing semaphores so as to facilitate coordination and mutual exclusion of operations by said at least two microprocessors.

5 17. The system of claim 1, further comprising a hardware control library loaded on a general purpose microprocessor of said processing module, said hardware control library comprising a set of functions for programming the parallel pipelined video hardware of said at least one video processing module to perform predetermined processing operations.

10 18. The system of claim 17, wherein said processing module comprises at least two general purpose microprocessors and said hardware control library further comprises a set of functions for coordinating multitask processing operations of said at least two general purpose microprocessors.

15 19. The system of claim 17, wherein said control data comprises video device information for each hardware component of said video processing system, wherein said functions of said hardware control library manipulate said video device information to program said hardware components for each of said different video processing operations.

20 20. A method of creating a modular video processing system, comprising the steps of:

connecting to a global control bus a processing module containing at least one general purpose microprocessor which controls hardware and software operation of said video processing system using control data;

25 connecting to said global control bus at least one video processing module which contains parallel pipelined video hardware which is programmable by said control data to provide different video processing operations on an input stream of video data;

said processing module detecting the presence of each video processing module connected to said global control bus; and

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said processing module passing said control data to each detected video processing module over said global control bus to program said parallel pipelined video hardware to perform a video processing function which is unique to particular processing tasks of said video processing system.

5 21. The method of claim 20, comprising the additional steps of coupling to a global video bus said video data with associated video timing information synchronized to a system clock, and routing said video data and its associated video timing information to/from respective parallel pipelined video hardware components of said video processing module over said global video bus via a crosspoint switch, said 10 timing data compensating for pipeline delay in said video processing module.

22. The method of claim 21, comprising the additional step of said processing module providing at least one synchronous start signal to each detected video processing module over said global control bus.

15 23. The method of claim 22, comprising the additional step of coordinating multitask processing operations when said processing module comprises at least two general purpose microprocessors.

24. The method of claim 21, comprising the additional steps of monitoring transfers of video data over each data path of said crosspoint switch and facilitating selection of idle data paths for each transfer of data from one parallel pipelined video 20 hardware component to another.

25. The method of claim 21, wherein said control data comprises video device information for each hardware component of said video processing system, comprising the further step of said processing module manipulating said video device information to program said hardware components for each of said different video 25 processing operations.

26. The method of claim 21, comprising the steps of automatically compensating for differences in input video timing between respective images and providing dual image pointwise video processing operations and image accumulations of said respective images.

5 27. A modular processing system comprising:

at least one specialized processing module which contains parallel pipelined hardware which is programmable to provide different specialized processing operations on an input stream of data;

10 a general processing module containing a general purpose microprocessor which controls hardware and software operation of said specialized processing module using a hardware control library loaded on said general purpose microprocessor, said hardware control library comprising a set of functions for programming said parallel pipelined hardware of said at least one specialized processing module to perform predetermined specialized processing operations; and

15 a global control bus which provides control data to/from said hardware control library of said general processing module from/to said at least one specialized processing module separate from said input data to be processed by said general processing module and said at least one specialized processing module.

28. The system of claim 27, wherein said input data is coupled with
20 associated timing information synchronized to a system clock, and each specialized
processing module comprises a crosspoint switch which routes said input data and its
associated timing information to/from respective parallel pipelined hardware
components, said timing data compensating for pipeline delay in said specialized
processing module.

25 29. The system of claim 27, wherein said general processing module
comprises at least two general purpose microprocessors and said hardware control
library further comprises a set of functions for coordinating multitask processing
operations of said at least two general purpose microprocessors.

30. The system of claim 27, wherein said hardware control library includes device information for each hardware component of said specialized processing system, wherein said functions of said hardware control library manipulate said device information to program said hardware components for each of said different specialized

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